AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please amend claims 1, 3 – 7, 9, 10, 15, 18, 26, and 27, inclusive, and cancel claims 2, 8, 11 and 28, as follows:

Listing of Claims:

1 (Currently Amended). A memory controller for ~~in~~ an adaptable computing circuit, the adaptable computing circuit having a programmable network and couplable to a memory, ~~machine (ACM),~~ the controller comprising:

a network interface configured to receive a memory request from the ~~a~~ programmable network and to send data to and receive data from the programmable network; ~~and~~

a memory interface configured to access a memory to fulfill the memory request; and ~~request from the programmable network,~~

at least one memory processing circuit coupled to the network interface and to the memory interface, the memory processing circuit configured to provide a memory access service of a plurality of memory access services,

wherein the memory interface receives and provides data for the memory request using the memory access service. ~~to the network interface, the network interface configured to send data to and receive data from the programmable network~~.

2. (Cancelled)

3 (Currently Amended). The controller of claim 1, ~~claim 2,~~ wherein the plurality of memory access services comprise at least one of a retrieve/write ("peek/poke") service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service.

4 (Currently Amended). The controller of claim 1, wherein the memory interface comprises at least one of a SDRAM interface and a flash memory interface.

5 (Currently Amended). The controller of claim 1, wherein the network interface is further configured to provide ~~provides~~ flow control with a node that has sent the memory request.

6 (Currently Amended). A memory controller for ~~in~~ an adaptable computing circuit, the adaptable computing circuit having an interconnection network coupled to a plurality of nodes, ~~machine (ACM),~~ the controller comprising:

a network interface configured to receive a memory request for a memory access service from ~~a~~ the interconnection network; and

a memory processing circuit ~~one or more engines~~ configured to receive the memory request and to provide a ~~the~~ memory access service of a plurality of memory access services, the memory access service associated with the memory request, and wherein the plurality of memory access services comprise at least one of a retrieve/write ("peek/poke") service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service.

7 (Currently Amended). The controller of claim 6, wherein the memory processing circuit comprises at least one of a ~~one or more engines comprise a~~ retrieve/write ("peek/poke") circuit, ~~engine,~~ a memory random access circuit, ~~engine,~~ a point-to-point circuit, ~~engine,~~ a direct memory access circuit, ~~engine,~~ and a real-time input circuit. ~~engine.~~

8 (Cancelled).

9 (Currently Amended). The controller of claim 6, wherein the network interface is further configured to provide data ~~provides~~ flow control with a node of the plurality of nodes that has sent the memory request.

10 (Currently Amended). A memory controller in an adaptable computing circuit, ~~machine (ACM),~~ the controller comprising:

one or more ports configured to receive memory requests, wherein each port includes one or more parameters;

a memory processing circuit ~~an engine~~ configured to receive a memory request from a port in the one or more ports; and

a data address generator configured to generate a memory location for a memory based on the one or more parameters associated with the port,

wherein the memory processing circuit is further ~~engine is~~ configured to perform a memory operation for the memory request using the generated memory location, the memory processing circuit comprising a processing circuit to perform at least one of point-to-point memory requests, direct memory access memory requests, and real-time input memory requests.

11 (Cancelled).

12 (Original). The controller of claim 10, wherein the data address generator is configured by the one or more parameters associated with the port.

13 (Original). The controller of claim 10, wherein the memory operation comprises at least one of a read and a write operation.

14 (Original). The controller of claim 10, wherein the memory location comprises one or more addresses.

15 (Currently Amended). The controller of claim 10, wherein the data address generator is further configured to use ~~uses~~ an initial location determined from the memory request to determine the memory location.

16 (Original). The controller of claim 15, wherein the initial location comprises a base address and an offset is used to determine the memory location.

17 (Original). The controller of claim 10, wherein the engine is configured to perform the memory operation while conforming to a point-to-point protocol with a requesting node that sent the memory request.

18 (Currently Amended). A memory controller in an adaptable computing circuit ~~machine (ACM), the node~~ the controller comprising:

one or more ports configured to receive memory requests from requesting nodes, wherein each port includes one or more parameters, the one or more parameters configurable by information in the memory requests;

a data address generator configured to generate a memory location for a memory based on the one or more parameters associated with the port; and

a point-to-point engine configured to receive a memory request from a port in the one or more ports and to perform a memory operation using the generated memory location while adhering to a point-to-point protocol with the requesting node. ;

~~a data address generator configured to generate a memory location for a memory based on the one or more parameters associated with the port,~~

~~wherein the point-to-point engine performs a memory operation using the generated memory location while adhering to a point-to-point protocol with the requesting node.~~

19 (Original). The controller of claim 18, wherein the memory request comprises:

at least one of a data request and a control request, wherein the data request includes data to be written and the control request includes information usable to update the one or more parameters.

20 (Original). The controller of claim 19, wherein the control request is included in a control word and the data request is included in a data word.

21 (Original). The controller of claim 19, wherein the control request includes data usable for configuring the one or more parameters associated with the port.

22 (Original). The controller of claim 21, wherein the control request includes an indication to perform a read after the one or more parameters have been configured.

23 (Original). The controller of claim 18, wherein the memory request includes a data request that includes data to be written in a memory.

24 (Original). The controller of claim 23, wherein the data is written into the memory using the one or more parameters associated with the port.

25 (Original). The controller of claim 24, wherein the memory location generated by the data address generator is used to write or read the data at that memory location in the memory.

26 (Currently Amended). The controller of claim 18, wherein the point-to-point engine and requesting node communicate using forward and backward acknowledgement messages ("ACKs") to maintain flow control.

27 (Currently Amended). A system for processing memory service requests in an adaptable computing environment, the system comprising:

a memory;

one or more nodes configured to generate a memory service request;

a memory controller configured to receive the memory service request, the memory controller configured to service the memory service request by reading data from or writing data ~~request, wherein the memory controller reads or writes data from or~~ to the memory based on the memory service request, and the memory controller further configured to provide at least one of a retrieve/write ("peek/poke") service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service.

28 (Cancelled).

29 (Original). The system of claim 27, wherein the memory comprises at least one of a SDRAM and Flash memory.

30 (Original). The system of claim 27, wherein the one or more nodes comprise an adaptable computing node.

31 (Original). The system of claim 27, wherein the memory controller comprises one or more ports, wherein each port in the one or more ports includes one or more parameters.

32 (Original). The system of claim 31, wherein the memory controller comprises a data address generator, the data address generator configured to use the one or more parameters associated with a port in the one or more ports to determine a location in the memory to read or write data.